PATENT ABSTRACTS

[** your application **]

8/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0015388572 & & *Drawing available*
WPI Acc no: 2005-733221/200575
XRPX Acc No: N2005-603623
Computer processor usage determining method, involves determining elapsed times between thread execution points based on start/stop times using profiler, and determining whether thread is idle during each time
Patent Assignee: FINDEISEN P (FIND-I)
Inventor: FINDEISEN P

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050229176	A1	20051013	US 2004805934	A	20040322	200575	B

Priority Applications (no., kind, date): US 2004805934 A 20040322

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050229176	A1	EN	11	4	

Alerting Abstract US A1
NOVELTY - The method involves determining elapsed times between thread execution points based on start/stop times associated with the points by a profiler. A determination is made whether a thread is idle during each elapsed time by comparing with a threshold value. The elapsed time during which the thread is idle is reduced to a value. A value indicative of processor usage by the thread is determined as a function of the elapsed times.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

a. a computer-readable medium configured with instructions for causing a processor of a data processing arrangement to perform a method for determining processor usage by a thread
b. an apparatus for determining processor usage by a thread.

USE - Used for determining a computer processor usage by a thread.
ADVANTAGE - The profiler provides accurate performance measurements on a thread-by-thread basis, thus efficiently determining processor usage by a thread.
DESCRIPTION OF DRAWINGS - The drawing shows a flow chart explaining steps in a thread profiling method.

12/5/2 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0016970844 & & *Drawing available*
WPI Acc no: 2007-685910/200764
Related WPI Acc No: 2002-054895
XRPX Acc No: N2007-538313
Operation method of computing system e.g. for notebook computer, involves adjusting clock throttle rate for CPU depending on its measured usage
Patent Assignee: MICROCONNECT LLC (MICR-N)
Inventor: LEE S H; OH J G

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20070106917	A1	20070510	US 2001850059	A	20010508	200764	B
			US 2006589280	A	20061030		

Priority Applications (no., kind, date): KR 200025787 A 20000515

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20070106917	A1	EN	9	4	Continuation of application	US 2001850059
					Continuation of patent	US 7131016

Alerting Abstract US A1
NOVELTY - The usage of the CPU is calculated by measuring its idle thread value for a set period of time or by detecting the CPU usage from the registry information of the system. The measured usage is compared with set minimum and maximum references. If the usage is between the minimum and maximum usages, the clock throttle rate is maintained. If the usage is less than the minimum, the clock rate is reduced and if the usage is more than the reference, the clock throttle rate is initialized.
DESCRIPTION - An INDEPENDENT CLAIM is included for a computing system.
USE - For operating computer e.g. personal computer (PC) with a single CPU (claimed), like desktop computer, notebook computer, etc.
ADVANTAGE - The electric power consumption is reduced without having any influence on the performance of the computer. The clock rate is adjusted and maintained for improved performance of the system.
DESCRIPTION OF DRAWINGS - The figure shows a flowchart explaining adjustment of clock throttle rate of the CPU.

12/5/8 (Item 7 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014630629 & & *Drawing available*
WPI Acc no: 2004-812627/200480
XRPX Acc No: N2004-641210
Processor time usage accounting method for simultaneous multi-threaded processor, involves updating processor resource usage counts in response to determination of resource usage of threads executing within processor
Patent Assignee: IBM UK LTD (IBMC); INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: ARMSTRONG W; ARMSTRONG W J; FLOYD M; FLOYD M S; KALLA R; KALLA R N; LEITNER L; LEITNER L S; LOYD M S; SINHAROY B

Patent Family (13 patents, 107 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040216113	A1	20041028	US 2003422025	A	20030423	200480	B
WO 2004095282	A1	20041104	WO 1586	A	20040414	200480	E
EP 1616259	A1	20060118	EP 2004727310	A	20040414	200606	E
			WO 1586	A	20040414		
BR 200409710	A	20060502	BR 2004009710	A	20040414	200634	E
			WO 1586	A	20040414		
MX 2005011307	A1	20060101	WO 1586	A	20040414	200637	E
			MX 0511307	A	20051021		
KR 2006002842	A	20060109	WO 1586	A	20040414	200659	E
			KR 717727	A	20050922		
JP 2006524380	W	20061026	WO 1586	A	20040414	200670	E
			JP 2006506116	A	20040414		
EP 1616259	B1	20070606	EP 2004727310	A	20040414	200738	E
			WO 1586	A	20040414		
DE 602004006858	E	20070719	DE 6858	A	20040414	200755	E
			EP 2004727310	A	20040414		
			WO 1586	A	20040414		
CN 1985242	A	20070620	CN 80001642	A	20040414	200774	E
			WO 1586	A	20040414		
ES 2286630	T3	20071201	EP 2004727310	A	20040414	200782	E
IN 200505346	P1	20071102	WO 1586	A	20040414	200812	E
			IN 5346	A	20051122		
DE 602004006858	T2	20080214	DE 6858	A	20040414	200815	E
			EP 2004727310	A	20040414		
			WO 1586	A	20040414		

Priority Applications (no., kind, date): US 2003422025 A 20030423

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040216113	A1	EN	10	4		
WO 2004095282	A1	EN				
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US					

	UZ VC VN YU ZA ZM ZW					
Regional Designated States,Original	AT BE BG BW CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PL PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW					
EP 1616259	A1	EN			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
Regional Designated States,Original	AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IT LI LT LU LV MC MK NL PL PT RO SE SI SK TR					
BR 200409710	A	PT			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
MX 2005011307	A1	ES			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
KR 2006002842	A	KO			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
JP 2006524380	W	JA	24		PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
EP 1616259	B1	EN			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
Regional Designated States,Original	AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PL PT RO SE SI SK TR					
DE 602004006858	E	DE			Application	EP 2004727310
					PCT Application	WO 1586
					Based on OPI patent	EP 1616259
					Based on OPI patent	WO 2004095282
CN 1985242	A	ZH			PCT Application	WO 1586
					Based on OPI patent	WO 2004095282
ES 2286630	T3	ES			Application	EP 2004727310
					Based on OPI patent	EP 1616259
IN 200505346	P1	EN			PCT Application	WO 1586
DE 602004006858	T2	DE			Application	EP 2004727310
					PCT Application	WO 1586
					Based on OPI patent	EP 1616259
					Based on OPI patent	WO 2004095282

Alerting Abstract US A1

NOVELTY - The method involves determining a relative resource usage of threads executing within a processor at a periodic interval. Multiple processor resource usage counts are updated in response to the determination of the resource usage. Each count is associated with a particular thread in conformity with the relative resource usage. A number of resources are determined for which the threads are in a particular cycle state.

DESCRIPTION - An INDEPENDENT CLAIM is also included for a simultaneous multi-threaded processor of supporting concurrent execution of a number of threads.

USE - Used for accounting a processor time usage in a simultaneous multi-threaded (SMT) processor.

ADVANTAGE - The method updates the processor resource usage counts in response to the determination of the relative resource usage, thus improving the efficiency of the simultaneous multi-threaded processor.

DESCRIPTION OF DRAWINGS - The drawing shows a flowchart depicting a method for accounting a processor time usage in a simultaneous multi-threaded (SMT) processor.

12/5/9 (Item 8 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014020432 & & *Drawing available*
WPI Acc no: 2004-202115/200419
Related WPI Acc No: 2005-046832
XRPX Acc No: N2004-160652
Hardware based utilization metering device for computer system, has counter coupled to state indicator and system clock for receiving data related to indication when processor is in one state to generate counter value
Patent Assignee: CIRCENIS E (CIRC-I); HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: CIRCENIS E; CIRCENIS E I

Patent Family (6 patents, 4 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040019456	A1	20040129	US 2002200175	A	20020723	200419	B
DE 10318622	A1	20040226	DE 10318622	A	20030424	200419	E
JP 2004054932	A	20040219	JP 2003181951	A	20030626	200419	E
GB 2393292	A	20040324	GB 200316794	A	20030717	200422	E
US 6816809	B2	20041109	US 2002200175	A	20020723	200474	E
GB 2393292	B	20051130	GB 200316794	A	20030717	200578	E

Priority Applications (no., kind, date): US 2002200175 A 20020723

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040019456	A1	EN	12	4		
JP 2004054932	A	JA	11			

Alerting Abstract US A1
NOVELTY - The device has a state indicator receiving an indication when a processor is in a state. A counter (140) coupled to the indicator and a system clock (130) receives a measure of system time. The counter also receives data related to the indication when the processor is in the state to generate a counter value. A data usage provider coupled to the counter provides the value.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

c. a hardware based method for measuring power utilization in a computer system
d. an apparatus that provides hardware based utilization metering of CPU.

USE - Used for measuring processor utilization in a computer system.
ADVANTAGE - The device accurately measures processor utilization and is capable of independently communicating with each operating system.
DESCRIPTION OF DRAWINGS - The drawing shows a basic block diagram of a system that meters CPU utilization data in a computer system running multiple instances of operating systems.
100 Computer system
120 Idle indicator
130 System clock
140 Counter
150 Usage data provider

12/5/10 (Item 9 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0013458846 & & *Drawing available*
WPI Acc no: 2003-550338/200352
XRPX Acc No: N2003-437649
Multiprocessor control program for computer, releases processor waiting state when number of upper limits of attribute of execution unit exceeds number of execution operations of processor
Patent Assignee: FUJITSU LTD (FUIT); PFU KK (USAE)
Inventor: FUJII Y; INDEN Y; KAMIO S; MATSUSHITA A; MIYAGAWA O; TAKADA K; TAMURA H

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 2003186856	A	20030704	JP 2001384027	A	20011218	200352	B

Priority Applications (no., kind, date): JP 2001384027 A 20011218

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 2003186856	A	JA	12	13	

Alerting Abstract JP A
NOVELTY - Waiting state of the processors (16a-16f) is released when the number of upper limits corresponding to the attribute of the execution unit (15g) acquired from a table (12) is more than the number of execution operations performed by the processor.
DESCRIPTION - An INDEPENDENT CLAIM is also included for multiprocessor control method.
USE - Multiprocessor control program for computer.
ADVANTAGE - Restrains the reduction of usage effectiveness of the processor and the reduction of parallel operation property of the processors.
DESCRIPTION OF DRAWINGS - The figure shows the theoretical diagram of the computer. (Drawing includes non-English language text).
1 computer
11 number of upper limits acquisition unit
12 table
13 execution number acquisition unit
14,15a-15h execution units
16a-16f processors

12/5/17 (Item 16 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008788176 & & *Drawing available*
WPI Acc no: 1998-332574/199829
XRPX Acc No: N1998-259594
Measurement method for of usage of resources by precess aid subsystems - CPU/s is periodically sampled to determine whether idle or busy and if busy the measurement of resource usage of terminated processes is corrected
Patent Assignee: BGS SYSTEMS INC (BGSS-N); BMC SOFTWARE INC (BMCS-N)
Inventor: AGRAWAL S C; NEWMAN K; RATHROCK C; ROTHROCK C

Patent Family (6 patents, 75 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5761091	A	19980602	US 1996763187	A	19961210	199829	B
WO 1998026351	A2	19980618	WO 1997IB1442	A	19971117	199830	E
AU 199747916	A	19980703	AU 199747916	A	19971117	199847	E
EP 1038226	A2	20000927	EP 1997910584	A	19971117	200048	E
			WO 1997IB1442	A	19971117		
EP 1038226	B1	20040414	EP 1997910584	A	19971117	200426	E
			WO 1997IB1442	A	19971117		
DE 69728698	E	20040519	DE 69728698	A	19971117	200434	E
			EP 1997910584	A	19971117		
			WO 1997IB1442	A	19971117		

Priority Applications (no., kind, date): US 1996763187 A 19961210

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 5761091	A	EN	16	11		
WO 1998026351	A2	EN				
National Designated States,Original	AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW					
Regional Designated States,Original	AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 199747916	A	EN			Based on OPI patent	WO 1998026351
EP 1038226	A2	EN			PCT Application	WO 1997IB1442
					Based on OPI patent	WO 1998026351
Regional Designated States,Original	BE DE ES FI FR GB IE IT NL SE					
EP 1038226	B1	EN			PCT Application	WO 1997IB1442
					Based on OPI patent	WO 1998026351
Regional Designated States,Original	BE DE ES FI FR GB IE IT NL SE					
DE 69728698	E	DE			Application	EP 1997910584
					PCT Application	WO 1997IB1442
					Based on OPI patent	EP 1038226
					Based on OPI patent	WO 1998026351

Alerting Abstract US A

The method involves measuring the resource usage, by the operating system processes of the computer system, by periodically sampling the CPU(s) to determine whether idle or apparently busy. If busy, with the process the measurement of resource usage of terminated processes is corrected.

The resource usage is measured by one or more process-implemented subsystems of the computer system by periodic sampling. The measurements taken by the subsystems are correlated with those taken by the operating system as corrected.

USE - Resources such as CPU's, memory, hard disks and network bandwidth by computer system processes, for such purposes as performance analysis and planning.

ADVANTAGE - Reduces errors.

12/5/18 (Item 17 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008061774 & & *Drawing available*
WPI Acc no: 1997-157341/199715
XRPX Acc No: N1997-129875
Computer data processing system with workload usage measuring capability - running cycle soaker task when CPU is not performing workload task, measuring total cycles run by CPU for task, and subtracting soaker cycles from total cycles
Patent Assignee: FULLER B (FULL-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: FULLER B

Patent Family (5 patents, 7 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 762286	A1	19970312	EP 1996650034	A	19960801	199715	B
JP 9134299	A	19970520	JP 1996223727	A	19960826	199730	E
US 5797115	A	19980818	US 1995518668	A	19950824	199840	E
EP 762286	B1	20000223	EP 1996650034	A	19960801	200015	E
DE 69606745	E	20000330	DE 69606745	A	19960801	200023	E
			EP 1996650034	A	19960801		

Priority Applications (no., kind, date): US 1995518668 A 19950824

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 762286	A1	EN	12	7		
Regional Designated States,Original	DE FR GB IT NL					
JP 9134299	A	JA	12			
EP 762286	B1	EN				
Regional Designated States,Original	DE FR GB IT NL					
DE 69606745	E	DE			Application	EP 1996650034
					Based on OPI patent	EP 762286

Alerting Abstract EP A1
The method measures central processing unit (CPU) (3) usage required to execute a predetermined workload that includes system overhead usage of the CPU as well as direct usage of the CPU. The CPU is driven to run processing cycles to perform a workload task (22) or to perform a cycle soaker task. A cycle soaker task runs directly on the CPU and has no system overhead.
The cycle soaker task runs whenever there is no workload task ready to run. A monitor module measures (28) the total of all cycles run and soaker cycles run by the CPU from beginning to end of execution of the workload. CPU usage attributable to the workload is measured (30) by deducting the soaker cycles from the total of all cycles.
ADVANTAGE - Quick and efficient way to manage computing system.

12/5/20 (Item 19 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0006173229 & & *Drawing available*
WPI Acc no: 1992-417436/199251
XRPX Acc No: N1992-318334
Resource usage monitoring for data processing system - displays performance statistics of system as number of graphical child windows contained in main window in OS/2 formats
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DEWITT J E; EMRICK S L; HOLCK T M; SUMMERS J H

Patent Family (4 patents, 4 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 518574	A2	19921216	EP 1992305195	A	19920605	199251	B
EP 518574	A3	19930825	EP 1992305195	A	19920605	199508	E
US 5463775	A	19951031	US 1991713484	A	19910610	199549	E
			US 1994263153	A	19940620		
US 5572672	A	19961105	US 1991713484	A	19910610	199650	E
			US 1994263153	A	19940620		
			US 1995500656	A	19950712		

Priority Applications (no., kind, date): US 1991713484 A 19910610; US 1994263153 A 19940620; US 1995500656 A 19950712

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 518574	A2	EN	50	14		
Regional Designated States,Original	DE FR GB IT					
EP 518574	A3	EN				
US 5463775	A	EN	41	14	Continuation of application	US 1991713484
US 5572672	A	EN	38	14	Continuation of application	US 1991713484
					Continuation of application	US 1994263153
					Continuation of patent	US 5463775

Alerting Abstract EP A2
The resource usage monitor for a data processing system includes a Data Collection Facility (DCF) and a Resource Monitor (RM). The DCF produces data on CPU time usage, Device usage and working memory use. This data is passed via an Applications interface (API) through a pipe to the RM.
The resource monitor uses OS/2 Presentation Manager windows and graphics functions to present one main window with a number of child windows. The child windows display data for one of the resources monitored. The user can control whether the display is historic or current (real-time).
ADVANTAGE - Provides real-time presentation of performance of various parts of data processing system.

[** bad date, but fyi **]

17/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0017149038 & & *Drawing available*
WPI Acc no: 2007-863986/200780
XRPX Acc No: N2007-687026
CPU time usage determining method for e.g. code refinement, involves determining current value of timer set for task, and subtracting current value from saved value to determine amount of elapsed processor time during interval
Patent Assignee: IBM UK LTD (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: GREINER D; GREINER D F

Patent Family (5 patents, 118 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
GB 2438230	A	20071121	GB 25722	A	20061221	200780	B
EP 1860567	A1	20071128	EP 2006126643	A	20061220	200780	E
US 20070271566	A1	20071122	US 2006437220	A	20060519	200780	E
WO 2007134648	A1	20071129	WO 69992	A	20061220	200780	E
GB 2440216	A	20080123	GB 25722	A	20061221	200814	E
			GB 9372	A	20070516		

Priority Applications (no., kind, date): US 2006437220 A 20060519

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
GB 2438230	A	EN	22	7		
EP 1860567	A1	EN				
Regional Designated States,Original	AL AT BA BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK NL PL PT RO SE SI SK TR YU					
WO 2007134648	A1	EN				
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM GT HN HR HU ID IL IN IS JP KE KG KM KN KP KR KZ LA LC LK LR LS LT LU LV LY MA MD MG MK MN MW MX MY MZ NA NG NI NO NZ OM PG PH PL PT RO RS RU SC SD SE SG SK SL SM SV SY TJ TM TN TR TT TZ UA UG US UZ VC VN ZA ZM ZW					
Regional Designated States,Original	AT BE BG BW CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IS IT KE LS LT LU LV MC MW MZ NA NL OA PL PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW					
GB 2440216	A	EN			Division of application	GB 25722

Alerting Abstract GB A
NOVELTY - The method involves executing a set CPU timer control instruction to set a value of a CPU timer. A task of a processing environment for which usage of CPU time is determined, is selected. A store CPU time control instruction is executed to save the value of the CPU timer. An amount of the CPU time used by the task is determined within a particular time interval. A current value of a timer set for the task is determined, and the current value is subtracted from the saved value to determine an amount of elapsed processor time used by the task during the interval.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a system comprising a unit to perform a method for determining CPU time usage.

USE - Used for determining CPU net time usage of a task e.g. job such as code refinement and billing, process and subroutine, of a processing environment.
ADVANTAGE - The method allows efficient determination of the CPU time usage of the task e.g. subroutine, of the processing environment, without calling operating system services.
DESCRIPTION OF DRAWINGS - The drawing shows a flow chart of a method of determining CPU time usage of tasks.

23/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0016213105 & & *Drawing available*
WPI Acc no: 2006-744748/200676
Related WPI Acc No: 2002-303311; 2005-064155; 2006-478909
XRPX Acc No: N2006-578222
Resource utilization measurement method for personal computer, involves adding execution times of threads which are not system threads and updating operating system register
Patent Assignee: MICROCONNECT LLC (MICR-N)
Inventor: LEE S H; OH J K

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20060212269	A1	20060921	US 2001930447	A	20010816	200676	B
			US 2004879091	A	20040630		
			US 2005240634	A	20051003		
			US 2006410834	A	20060426		

Priority Applications (no., kind, date): KR 200050037 A 20000828

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20060212269	A1	EN	6	2	Continuation of application	US 2001930447
					Continuation of application	US 2004879091
					Continuation of application	US 2005240634
					Continuation of patent	US 6804630
					Continuation of patent	US 7010466

Alerting Abstract US A1
NOVELTY - A Microsoft windows (RTM: not defined) operating system (OS) register containing processor usage information, is provided. The time required by a processor to execute threads during predetermined time interval is read using manager functions. The execution times of the threads which are not system threads, is totaled so as to determine the quantity of usage of the processor, and the OS register is updated accordingly.
DESCRIPTION - An INDEPENDENT CLAIM is included for operating system register update method.
USE - For measuring quantity of usage of system resource such as CPU of personal computer (PC).
ADVANTAGE - The quantity of usage of CPU is measured in short time without degrading the performance of the operating system. Power consumption is decreased by adjusting the clock pulse of CPU appropriately according to the usage.
DESCRIPTION OF DRAWINGS - The figure shows the flowchart explaining the resource utilization measurement method of personal computer.

23/5/9 (Item 9 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014716538 & & *Drawing available*
WPI Acc no: 2005-064155/200507
Related WPI Acc No: 2002-303311; 2006-478909; 2006-744748
XRPX Acc No: N2005-055594
CPU usage quantity measuring method for computer, has subtracting total execution time for previously stored thread from grand total, and measuring quantity by dividing subtracted time by timer time using virtual machine manager
Patent Assignee: LG ELECTRONICS INC (GLDS); MICROCONNECT LLC (MICR-N)
Inventor: LEE S H; OH J K

Patent Family (2 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040254765	A1	20041216	US 2001930447	A	20010816	200507	B
			US 2004879091	A	20040630		
US 7010466	B2	20060307	US 2004879091	A	20040630	200618	E

Priority Applications (no., kind, date): KR 200050037 A 20000828; US 2004879091 A 20040630

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040254765	A1	EN	6	2	Continuation of application	US 2001930447
					Continuation of patent	US 6804630

Alerting Abstract US A1
NOVELTY - The method involves reading execution time of all threads excluding a system thread with a certain timer time interval, and adding the read time to obtain a grand total. A total execution time for a previously stored thread is read. The total execution time for the stored thread is subtracted from the grand total. A quantity of usage is got by dividing the subtracted time by the timer time, using a virtual machine manager.
USE - Used for measuring a quantity of usage of a CPU of a computer.
ADVANTAGE - The method uses the virtual machine manager provided by MS-Windows, such that there is no need to amend an algorithm in order to adapt it for the other MS-Windows nor does it require a complicated code. The method is very useful for application monitoring and reporting of a load of the CPU in accordance with an operation state of the computer.
DESCRIPTION OF DRAWINGS - The drawing shows a flow chart illustrating a method for measuring a quantity of usage of a CPU.

23/5/11 (Item 11 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0013887757 & & *Drawing available*
WPI Acc no: 2004-066896/200407
XRPX Acc No: N2004-054307
Memory usage monitoring method for computer system, involves calculating time zone when CPU load reduces just before attainment time at which memory usage reaches threshold value and recovering memory leak
Patent Assignee: HITACHI JOHO SEIGYO SYSTEM KK (HITA-N); HITACHI LTD (HITA)
Inventor: HORIE M; KAIRA K; NAKABASHI A; NAKANO T; TOTSUGI K

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 2004005305	A	20040108	JP 2002161060	A	20020603	200407	B

Priority Applications (no., kind, date): JP 2002161060 A 20020603

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
JP 2004005305	A	JA	9	6	

Alerting Abstract JP A
NOVELTY - The memory usage and CPU load of the computer system are acquired regularly and stored in time series with the acquisition time. The attainment time at which the memory usage reaches the threshold value, is estimated based on the time series data. The time zone when the CPU load reduces just before the attainment time, is calculated based on time series of the CPU load and memory leak recovery is performed in the time zone.
DESCRIPTION - An INDEPENDENT CLAIM is also included for computer system.
USE - For recovering reduction of processing responsiveness by computer deadlock, memory leak, slashing of computer system.
ADVANTAGE - Enables the computer system to operate stably, by performing recovery processing before threshold.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the computer system. (Drawing includes non-English language text).
101 operating system managed table
102 information acquisition processor
103 memory load log information area
104 CPU load log information area
105 information analysis processor
106 recovery processing execution unit

23/5/23 (Item 23 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008684448 & & *Drawing available*
WPI Acc no: 1998-223678/199820
XRPX Acc No: N1998-177534
Subscriber accommodation load automatic regulation system of stored program control exchange - provides movement process notification to subscriber moving management unit such that usage efficiency of all processors is within limits of equalisation threshold
Patent Assignee: NEC CORP (NIDE)
Inventor: MITSUI T

Patent Family (2 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 10065798	A	19980306	JP 1996213775	A	19960813	199820	B
JP 3064920	B2	20000712	JP 1996213775	A	19960813	200038	E

Priority Applications (no., kind, date): JP 1996213775 A 19960813

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
JP 10065798	A	JA	5	3		
JP 3064920	B2	JA	5		Previously issued patent	JP 10065798

Alerting Abstract JP A
The system has a processor usage efficiency management unit (1) that measures the usage efficiency of several processors and provides a notification to a threshold management unit (2) within a predetermined timing. The threshold management unit distinguishes whether the obtained value is within the limits of usage efficiency set up beforehand.
When the usage efficiency is out of the range of equalisation threshold, a notification is given to a subscriber registration deletion unit (3). The movement process notification is done to a subscriber moving management unit (4) such that the usage efficiency of all the processors is within the limits of the equalisation threshold.
ADVANTAGE - Maintains balance of usage efficiency of each processor. Removes disadvantage of load distribution system.

FULL-TEXT PATENTS

12/3K/2 (Item 2 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01608141
Method and apparatus for balancing load in a computer system
Verfahren und Vorrichtung zur Lastverteilung in einem Rechnersystem
Procede et dispositif pour repartir la charge dans un systeme d'ordinateur

Patent Assignee:

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(Applicant designated States: all)

Inventor:

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Milan Court, Bird Hall Lane, Cheadle Heath; Stockport, Cheshire SK3 0WY; (GB)

Legal Representative:

g. Brandon, Paul Laurence et al (75051)
APPLEYARD LEES, 15 Clare Road; Halifax HX1 2HY; (GB)

	Country	Number	Kind	Date	
Patent	EP	1329811	A2	20030723	(Basic)
	EP	1329811	A3	20040818	
	EP	1329811	A3	20040818	
Application	EP	2002258408		20021205	
Priorities	GB	129221		20011206	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LI; LU; MC; NL;
PT; SE; SI; SK; TR;

Extended Designated States:
AL; LT; LV; MK; RO;

International Patent Class (V7): G06F-009/50; G06F-011/34; G06F-001/32Abstract Word Count: 59
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200330	416
SPEC A	(English)	200330	2792
Total Word Count (Document A) 3208			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 3208			

Specification: ...reducing the CPU usage from at least one CPU demand source, thereby to reduce the CPU load, if the CPU monitoring means determines that a predetermined threshold CPU usage is at... ...Suitably, a thread is clamped by limiting the amount of CPU capacity available to that thread. Suitably, a thread is clamped by temporarily suspending the relevant thread. Suitably, a thread is clamped by or to a predetermined percentage.

Suitably, the apparatus further comprises means for determining a thread to be clamped. Suitably, the thread determining means comprises means for determining the CPU usage of a process of which a thread forms a part and in which the CPU usage reducing means is only activated for the process if the CPU usage of the process at least reaches a predetermined threshold. Suitably, the thread determining means comprises means for determining the CPU usage of a thread and in which the CPU usage reducing means is only activated for the thread if the CPU usage of the thread at least reaches a predetermined threshold.

Suitably, the computer apparatus is a terminal server for...Suitably, a thread is clamped by limiting the amount of CPU capacity available to that thread. Suitably, a thread is clamped by temporarily suspending the relevant thread. Suitably, a thread is clamped by or to a predetermined percentage.

Suitably, the apparatus further comprises means for determining a thread to be clamped. Suitably, the thread determining means comprises means for determining the CPU usage of a process of which a thread forms a part and in which the CPU usage reducing means is only activated for the process if the CPU usage of the process at least reaches a predetermined threshold. Suitably, the thread determining means comprises means for determining the CPU usage of a thread and in which the CPU usage reducing means is only activated for the thread if the CPU usage of the thread at least reaches a predetermined threshold.

According to the present invention in a fourth aspect, there is provided a performance management... ...usage from at least one user if the CPU usage at least reaches a predetermined threshold, in which the CPU usage is reduced by thread clamping.

Suitably, the terminal server comprises part of a server farm.

Suitably, the CPU usage is sampled at a predetermined rate.

Suitably, the predetermined threshold must be at least reached for a plurality of samples before the CPU usage is reduced.

Suitably, the predetermined threshold is 100% of the CPU capacity.

Suitably, a thread is clamped by temporarily suspending the... ...for the process if the CPU usage of the process at least reaches a predetermined threshold. Suitably, the method further comprises determining the CPU usage of a thread and in which the CPU usage is only reduced for the thread if the CPU usage of the thread at least reaches a predetermined threshold.

Suitably, a thread is clamped for a predetermined period.

Suitably, a user or group of users is allocated... ...reduced.

Suitably, after reducing CPU usage, if the CPU usage still at least reaches a predetermined value, CPU usage is further reduced until it is below a predetermined value.

The present invention extends to computer programs for carrying out such methods and to data...be required if for "samples(underscore)before clamping" samples the CPU load remains at the predetermined value of 100%. Other CPU usage may be set, to avoid usage reaching 100% if... ...a "sample(underscore)period" of 1 will instruct the performance manager 26 to start clamping threads if the system CPU load remains at 100% for three seconds.

If clamping is not... ...300). If, however, clamping is required, in step 304 it is determined which of the threads currently using CPU capacity is/are to be clamped.

Any given process may include a plurality of threads therein. To enable both processes and threads within them to be assessed for clamping, first the sampler determines whether the CPU load for a given process exceeds the "minimum(underscore)process CPU" value. If the "minimum(underscore)process CPU" value is not exceeded the performance manager 26 will not clamp the threads within that process regardless of the amount of CPU load the individual threads are using.

The performance manager will only clamp threads that are occupying a significant percentage of the CPU load. The performance manager compares the sampled CPU load for a given thread with the "minimum(underscore)process CPU" variable and will only clamp the corresponding thread if the CPU load exceeds that percentage.

Typical values for "minimum(underscore)process(underscore)cpu" and "minimum(underscore)thread(underscore)cpu" are 5%.

Once one or more threads has or have been determined to be clamped, the performance manager will (step 306) clamp the thread or threads by the "clamp(underscore)quantity" percentage of the CPU capacity for a predetermined period, being...

Claims: ...thereby to reduce the CPU load, if the CPU monitoring means determines that a predetermined threshold CPU usage is at least reached, in which the CPU usage reducing means comprises a... ...predetermined rate.

4. A computer apparatus according to any preceding claim, in which the predetermined threshold must be at least reached for a plurality of samples before the CPU usage reducing... ...at least one CPU demand source if the CPU usage at least reaches a predetermined threshold, in which the CPU usage is reduced by thread clamping.

6. A performance management method for a computer apparatus according to claim 5, in... ...for a computer apparatus according to claim 5 or claim 6, in which the predetermined threshold must be at least reached for a plurality of samples before the CPU usage is... ...a computer apparatus according to any one of claims 5 to 7, in which a thread is clamped for a predetermined period.

9. A terminal server apparatus comprising a terminal server... ...means for reducing the CPU usage from at least one user, thereby to reduce the CPU load, if the CPU monitoring means determines that a predetermined threshold CPU usage is at least reached, in which the CPU usage reducing means comprises a thread clamper.

12/3K/3 (Item 3 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01254488
Apparatus and methods for managing resource usage
Verfahren und Vorrichtung zum Verwalten der Verwendung eines Betriebsmittels
Procede et appareil pour la gestion de l'utilisation d'une ressource

Patent Assignee:

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(Applicant designated States: all)

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Legal Representative:

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Urquhart-Dykes & Lord Tower North Central Merrion Way; Leeds LS2 8PA; (GB)

	Country	Number	Kind	Date	
Patent	EP	1083485	A2	20010314	(Basic)
	EP	1083485	A3	20040225	
Application	EP	2000307736		20000907	
Priorities	US	394118		19990910	

Designated States:
DE; FR; GB;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-009/50Abstract Word Count: 81
NOTE: NONE
NOTE: Figure number on first page: NONE

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200111	1529
SPEC A	(English)	200111	5220
Total Word Count (Document A) 6749			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 6749			

Specification: ...present invention. Of course, a similar resource may also be managed with the procedure of Figure 4. Initially, the CPU or network usage is monitored for all threads associated with a resource context in operation 402. It is then determined whether a first threshold is exceeded in operation 404. If the first threshold is not exceeded, CPU or network usage continues to be monitored in operation 402.

If the first threshold is exceeded, the scheduler is instructed to lower the priority of the threads associated with the resource context in operation 406. The CPU or network usage is then monitored again for all the threads associated with the resource context in operation 408 to determine when to boost the priority back up. It is then determined whether resource usage has dropped below a second threshold in operation 410. Of course, a single threshold may be used to determine when to lower and boost the priority.

If usage has not dropped below the second threshold, it is then determined whether the first threshold is still exceeded in operation 412. If the first threshold is still exceeded, the scheduler is again instructed to lower the priority of the thread... ...with a particular resource context continues to be lowered as the long as the first threshold is still exceeded. If the first threshold is not exceeded, the CPU or network usage is then monitored again for all the...

Claims: ...medium as recited in claim 23 further comprising:

computer code for associating a plurality of thresholds with the particular resource and the related code; and

computer code for notifying a registered particular resource by the related code exceeds a first one of the thresholds.

25. A computer readable medium as recited in claim 23 further comprising computer code for... ...of the particular resource by the related code drops below a second one of the thresholds that has a different value than the first threshold.

26. A computer readable medium as recited in any of claims 20-22 wherein the particular resource is CPU usage or network usage.

27. A computer readable medium as recited in claim 26 further comprising:

computer code for associating a threshold with the particular resource and the related code; and

computer code for indicating that the... ...the amount of resource usage of the particular resource by the related code exceeds the threshold.

28. A computer readable medium as recited in claim 27 further comprising:

computer code for associating a second threshold with the particular resource and the related code; and

computer code for indicating that the... ...of resource usage of the particular resource by the related code drops below the second threshold.

29. A method as recited in any of claims 20-28 wherein the related code is configured to be executed on behalf of an applet in the form of threads.

12/3K/4 (Item 4 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01011092
Method and apparatus for optimizing the execution of software applications
Verfahren und Gerat zur Optimierung des Programmablaufs von Anwendungen
Methode et appareil pour optimiser l'execution d'applications

Patent Assignee:

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(Proprietor designated states: all)

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Legal Representative:

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Urquhart-Dykes & Lord LLP Tower North Central Merrion Way; Leeds LS2 8PA; (GB)

	Country	Number	Kind	Date	
Patent	EP	908818	A2	19990414	(Basic)
	EP	908818	A3	20010620	
	EP	908818	B1	20060419	
Application	EP	98307744		19980924	
Priorities	US	944735		19971006	

Designated States:
DE; FR; GB; NL; SE;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-009/45

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G06F-0009/45	A	I	F	B	20060101	19990123	H	EP

Abstract Word Count: 114
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199915	1429
SPEC A	(English)	199915	6533
CLAIMS B	(English)	200616	1075

CLAIMS B	(German)	200616	1081
CLAIMS B	(French)	200616	1189
SPEC B	(English)	200616	6541
Total Word Count (Document A) 7963			
Total Word Count (Document B) 9886			
Total Word Count (All Documents) 17849			

Specification: ...reached an idle period involves determining whether a period of low activity has reached a threshold value, e.g., approximately 100 milliseconds or approximately half a second.

In general, the occurrence... ...Alternatively, the existence of an idle period may be determined by monitoring the status of threads associated with the overall computer system.

When CPU usage is monitored to identify periods of relative inactivity, CPU usage is essentially monitored to determine when the CPU usage falls below a certain usage threshold. The usage threshold, i.e., a "low activity threshold," may be widely varied. By way of example, the usage threshold may be set such that when substantially only activities with low overhead, such as setting... ...one embodiment, when CPU usage during the processing of the program falls below a usage threshold which is approximately 20 percent of the overall system resources, then the overall processing of... ...80 percent of the system resources may be available for use.

Monitoring the status of threads may involve studying a thread scheduler, as will be appreciated by those skilled in the art. When the thread scheduler indicates that all threads are blocked, i.e., substantially none of the threads are in a "run-able" state, then the implication is that the program is not...

Specification: ...on the order of a number of seconds, minutes, days or more.

In general, a threshold value is used to recognize a "useful" pause. For example, if the actual pause has lasted for a predetermined number of milliseconds, then the system may recognize the pause as a useful pause which is... ...reached an idle period involves determining whether a period of low activity has reached a threshold value, e.g., approximately 100 milliseconds or approximately half a second.

In general, the occurrence... ...Alternatively, the existence of an idle period may be determined by monitoring the status of threads associated with the overall computer system.

When CPU usage is monitored to identify periods of relative inactivity, CPU usage is essentially monitored to determine when the CPU usage falls below a certain usage threshold. The usage threshold, i.e., a "low activity threshold," may be widely varied. By way of example, the usage threshold may be set such that when substantially only activities with low overhead, such as setting... ...one embodiment, when CPU usage during the processing of the program falls below a usage threshold which is approximately 20 percent of the overall system resources, then the overall processing of... ...80 percent of the system resources may be available for use.

Monitoring the status of threads may involve studying a thread scheduler, as will be appreciated by those skilled in the art. When the thread scheduler indicates that all threads are blocked, i.e., substantially none of the threads are in a "run-able" state, then the implication is that the program is not...

NPL

8/5/1 (Item 1 from file: 2) Links
Fulltext available through: STIC Full Text Retrieval Options
INSPEC

07905070 INSPEC Abstract Number: C2001-05-5470-003
Title: A framework for performance evaluation based on event tracing
Author Horikawa, T.
Author Affiliation: C&C Media Res., NEC Corp., Japan
Journal: Transactions of the Information Processing Society of Japan vol.42, no.1 p. 68-78
Publisher: Inf. Process. Soc. Japan ,
Publication Date: Jan. 2001 Country of Publication: Japan
CODEN: JSGRD5 ISSN: 0387-5806
SICI: 0387-5806(200101)42:1L.68:FPEB;1-0
Material Identity Number: T205-2001-004

Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: A framework is described for establishing a formulated method of performance evaluation based on event tracing. It consists of abstractions representing a system, its behavior and the events to be measured. It also includes formulations of performance measures and of algorithms for obtaining them from an event trace. The measures include not only the usual ones, such as throughput, response time and resource utilization, but also those describing such process interactions as process waiting time and semi-busy waiting. The framework has been applied to the performance evaluation of an Apache HTTP server running on Linux 2.2.14 and 2.3.41 and executing the SPECweb96 benchmark program. This case study has clarified the differences between the two versions of Linux, including differences in CPU usage, global kernel lock usage, processing time and process switch frequency. The case study also indicates that Linux 2.2.14 has a performance bottleneck other than the physical resources, thus the measurement of CPU usage alone is not enough; we also need to consider object interactions, including inter-process communications, at least so far as Apache HTTP servers are concerned. (19 Refs)
Subfile: C
Descriptors: hypermedia; network servers; performance evaluation; transport protocols; Unix
Identifiers: performance evaluation framework; event tracing; abstractions; system behavior; performance measures; algorithms; throughput; response time; resource utilization; process interactions; process waiting time; semi-busy waiting; Apache HTTP server; Linux 2.2.14; Linux 2.3.41; SPECweb96 benchmark program; case study; CPU usage; global kernel lock usage; processing time; process switch frequency; performance bottleneck; object interactions; inter-process communications
Class Codes: C5470 (Performance evaluation and testing); C5630 (Networking equipment); C6150J (Operating systems)

16/5/3 (Item 1 from file: 23) Links
CSA Technology Research Database

0008881867 IP Accession No: 200804-71-464530; 200804-61-491888; 2008448921; A08-99-478695
Method for load balancing a per processor affinity scheduler wherein processes are strictly affinitized to processors and the migration of a process from an affinitized processor to another available processor is limited

Boland, Vernon K; Brasche, Kevin R; Smith, Kenneth A
, USA
Publisher Url: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u =/netaht ml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=58 72972.PN.&OS=pn/5872972& RS=PN/5872972

Document Type: Patent
Record Type: Abstract
Language: English
File Segment: Metadex; Mechanical & Transportation Engineering Abstracts; ANTE: Abstracts in New Technologies and Engineering; Aerospace & High Technology

Abstract:
An improved affinity process scheduling method for a multiprocessor computer system, wherein a process previously executed on a processor within the computer system is affined to the processor on which it previously executed, and will be scheduled for execution by the affined processor during subsequent requests for execution of the affined process. The improved affinity process scheduling method monitors the length of time the affined process resides on the system run queue awaiting execution by its affined processor; and schedules the affined process for execution with another available processor when the length of time the affined process has been waiting for execution exceeds a predetermined 'steal-age'threshold. The improved affinity process scheduling method also monitors the processing load borne by the affined processor, determines therefrom a headroom parameter for the affined processor, the headroom parameter indicating the remaining load capacity of the affined processor; and schedules the affined process for execution with another available processor when the headroom of the affined processor is less than a predetermined 'low-headroom'threshold.

Descriptors: Microprocessors; Affinity; Scheduling; Monitors; Schedules; Migration; Load balancing (computing); Queues; Load balancing; Multiprocessor
Subj Catg: 71, General and Nonclassified; 61, Design Principles; 99, General